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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,217	12/11/2003	Axel Brintzinger	2002 P 12234 US	8003

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,217	BRINTZINGER ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/733,217. Currently, claims 1-22 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

2. Claims 14 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation ***forming a plurality of conductors over the surface of the wafer in accordance with the patterning*** (claim 14, lines 3-4). The meaning of the phrase ***in accordance with the patterning*** is unclear.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto et al. (US 2002/0093082 A1 in view of Klocke et al. (US 2003/0079989 A1).

The Miyamoto et al. pre-grant published application (Miyamoto) discloses a method of forming a resist layer on a non-planar surface of a substrate (figs. 3, 8, 9, 11-13, 20-22 and pars. 102-121). The method comprises the steps of: providing a substrate 1 having a non-planar surface (fig. 9);[1] and forming a photoresist pattern 8 on the non-planar surface (fig. 12 and par. 110, lines 1-3).

The non-planar surface comprises a substantially planar surface with a structure 5 formed thereon (fig. 9 and par. 108, lines 1-9).

A conductive layer 7 is formed over the non-planar surface prior to forming the photoresist pattern 8, the conductive layer comprising a seed layer (fig. 11 and par. 109, lines 4-10).

A second conductive layer 9 is formed over portions of the seed layer not covered by the photoresist pattern (fig. 12 and par. 110, lines 1-5).

The substrate 1 comprises a semiconductor wafer (par. 102, lines 1-3). In addition, the second conductive layer 9 comprises a reroute layer 2 electrically coupling a contact pad BP formed on the semiconductor wafer to a terminal 14

[1] The photosensitive polyimide layer 5 forms a non-planar surface with the top surface of the substrate, wherein the substrate surface up to this step in the process includes the bond pad BP, the passivation layer 3, and the wiring layer 4.

on the non-planar surface (figs. 3, 22; par. 111, lines 1-5; and par. 121, lines 6-9).[2]

As explained above, Miyamoto discloses forming a photoresist pattern 8 on the non-planar surface. While Miyamoto discloses forming a photoresist pattern on the non-planar surface, Miyamoto does not disclose forming the photoresist by: placing the non-planar surface into an electrophoretic resist; applying an electrical voltage between the substrate and the electrophoretic resist, while the non-planar surface is in the electrophoretic resist; and removing the non-planar surface from the electrophoretic resist.

The Klocke et al. pre-grant published application (Klocke) discloses a method for depositing an electrophoretic resist on microelectronic workpieces for the fabrication of microelectronic devices (par. 9, lines 10-14). The electrophoretic resist is formed by: placing a workpiece into an electrophoretic resist; applying an electrical voltage between the substrate and the electrophoretic resist, while the workpiece is in the electrophoretic resist; and subsequently removing the workpiece from the electrophoretic resist (fig. 17; par. 91, lines 1-19; and par. 111, lines 1-3).

In one embodiment, the method further comprises protecting the rear surface of a workpiece from wetting while the workpiece is placed in the electrophoretic resist (par. 33, lines 12-18 and par. 48, lines 13-19).

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[2] The reroute layer 2 electrically couples the contact pad BP to the terminal 14 (i.e. solder bump 14) via bump lands 2A (figs. 3, 22 and par. 121, lines 6-9).

In one embodiment, the method further comprises causing the workpiece to be moved relative to the electrophoretic resist while the workpiece is placed in the electrophoretic resist (par. 49, 1-5; par. 51, 1-5; and par. 91, lines 9-19). The workpiece is rotated while the workpiece is placed in the electrophoretic resist (par. 49, 1-5; par. 51, 1-5; and par. 91, lines 9-19).

In one embodiment, the electrophoretic resist is stirred while the workpiece is placed in the electrophoretic resist (par. 49, lines 5-6).

The method further comprises heating the workpiece after removing the workpiece from the electrophoretic resist (par. 112, lines 8-18).

The substrate of Miyamoto has a highly topographical surface. One advantage of using an electrophoretic resist in place of a conventional photoresist is that an electrophoretic resist covers highly topographical surfaces with a conformal layer of material (Klocke – par. 31, lines 1-6). Thus, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Miyamoto by using an electrophoretic resist in place of the photoresist, as taught by Klocke, because an electrophoretic resist covers highly topographical surfaces with a conformal layer of material.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyamoto in view of Klocke as applied to claim 5 above, and further in view of Brintzinger et al. (US 2004/0087131 A1).

As explained above, Miyamoto discloses forming a second conductive layer 9 over portions of the seed layer not covered by the photoresist pattern. While forming the second conductive layer comprises forming a copper layer over portions of the seed layer not covered by the photoresist pattern, and forming a nickel layer over the copper layer (par. 110, lines 6-8), Miyamoto does not disclose forming a gold layer over the nickel layer.

The Brintzinger et al. pre-grant published application (Brintzinger) discloses forming a second conductive layer 5, 6, 7 over portions of a seed layer 4 (fig. 3 and par. 23, lines 1-9). The second conductive layer comprises a copper layer 5, a nickel layer 6 formed over the copper layer, and a gold layer 7 formed over the nickel layer (par. 23, lines 7-9).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Miyamoto and Klocke by forming a gold layer over the nickel, as taught by Brintzinger, since thee nickel layer must be coated with gold to achieve solderability (par. 5, lines 1-3).

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being obvious over Brintzinger in view of Klocke.

The applied reference, US 2004/0087131 A1, has a common assignee and at least one common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed

but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claims 1-12

The Brintzinger et al. pre-grant published application (Brintzinger) discloses a method of forming a resist layer on a non-planar surface of a substrate (figs. 1-6 and accompanying text). The method comprises: providing a substrate 1 having a non-planar surface (fig. 1 and par. 21, lines 1-3); and forming a photoresist pattern 10 on the non-planar surface (fig. 1 and par. 23, lines 4-5).

The non-planar surface comprises a substantially planar surface with a structure 2 formed thereon, the structure 2 comprising a compliant element (fig. 1 and par. 21, lines 1-3).

A conductive layer 4 is formed over the non-planar surface prior to forming the photoresist pattern 10, the conductive layer comprising a seed layer (fig. 1 and par. 23, lines 2-4).

A second conductive layer 5, 6, 7 is formed over portions of the seed layer 4 not covered by the photoresist pattern 10 (figs. 2, 3 and par. 23, lines 7-11). Forming the second conductive layer 5, 6, 7 comprises: forming a copper layer 5 over portions of the seed layer 4 not covered by the photoresist pattern 10, forming a nickel layer 6 over the copper layer, and forming a gold layer 7 over the nickel layer (figs. 2, 3 and par. 23, lines 7-11).

The second conductive layer 5, 6, 7 comprises a reroute layer (). As disclosed in the section entitled "Background Art," the purpose of the reroute layer is to electrically couple a contact pad formed on a semiconductor wafer (i.e. semiconductor chip) to a terminal (par. 2, lines 1-8). The terminal (not shown) is subsequently formed on the non-planar surface (par. 26, lines 3-4).

As explained above, Brintzinger discloses forming a photoresist pattern 10 on the non-planar surface. While Brintzinger discloses forming a photoresist pattern on the non-planar surface, Brintzinger does not disclose forming the photoresist by: placing the non-planar surface into an electrophoretic resist; applying an electrical voltage between the substrate and the electrophoretic resist, while the non-planar surface is in the electrophoretic resist; and removing the non-planar surface from the electrophoretic resist.

Klocke discloses a method for depositing an electrophoretic resist on microelectronic workpieces for the fabrication of microelectronic devices (par. 9, lines 10-14). The electrophoretic resist is formed by: placing a workpiece into an electrophoretic resist; applying an electrical voltage between the substrate and the electrophoretic resist, while the workpiece is in the electrophoretic resist; and subsequently removing the workpiece from the electrophoretic resist (fig. 17; par. 91, lines 1-19; and par. 111, lines 1-3).

In one embodiment, the method further comprises protecting the rear surface of a workpiece from wetting while the workpiece is placed in the electrophoretic resist (par. 33, lines 12-18 and par. 48, lines 13-19).

In one embodiment, the method further comprises causing the workpiece to be moved relative to the electrophoretic resist while the workpiece is placed in the electrophoretic resist (par. 49, 1-5; par. 51, 1-5; and par. 91, lines 9-19). The workpiece is rotated while the workpiece is placed in the electrophoretic resist (par. 49, 1-5; par. 51, 1-5; and par. 91, lines 9-19).

In one embodiment, the electrophoretic resist is stirred while the workpiece is placed in the electrophoretic resist (par. 49, lines 5-6).

The method further comprises heating the workpiece after removing the workpiece from the electrophoretic resist (par. 112, lines 8-18).

The structure of Brintzinger is a three dimensional (3D) structure (par. 21, lines 1-3). One advantage of using an electrophoretic resist in place of a conventional photoresist is that an electrophoretic resist is useful for

depositing a material on 3D structures because it covers highly topographical surfaces with a conformal layer of material (Klocke – par. 31, lines 1-6). Thus, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Brintzinger by using an electrophoretic resist in place of the photoresist, as taught by Klocke, because an electrophoretic resist covers highly topographical surfaces with a conformal layer of material.

Regarding Claims 13-22

Brintzinger discloses a method for forming a plurality of three-dimensional structures on a substrate (figs. 1-3 and accompanying text). The method comprises: providing a wafer 3 with bumps 2 distributed on a surface of the wafer (fig. 2 and par. 21, lines 1-3); and forming a resist over the surface of the wafer including the bumps by coating the surface of the wafer with a photoresist (par. 23, lines 4-5).

The method further comprises patterning the resist (par. 23, lines 4-5), and forming a plurality of conductors 5, 6, 7 over the surface of the wafer in accordance with the patterning (par. 23, lines 7-9).

The plurality of conductors electrically connects bonding pads on the wafer to terminals located on the bumps (par. 2, lines 1-8 and par. 26, lines 3-4).

Brintzinger does not disclose forming the resist by coating the surface of the wafer with an electrophoretic resist by dipping the surface of the wafer into the resist and by applying an electrical voltage between the wafer and the electrophoretic resist.

Klocke discloses a method for depositing an electrophoretic resist on microelectronic workpieces for the fabrication of microelectronic devices (par. 9, lines 10-14). The electrophoretic resist is formed by dipping the surface of the wafer into the resist and by applying an electrical voltage between the wafer and the electrophoretic resist (fig. 17; par. 91, lines 1-19; and par. 111, lines 1-3).

In one embodiment, the workpiece is dipped into the electrophoretic resist in a horizontal arrangement of the wafer (par. 33, lines 12-18 and par. 48, lines 13-19). A rear side of the workpiece is protected from wetting during the process of dipping into the electrophoretic resist (par. 33, lines 12-18 and par. 48, lines 13-19).

In one embodiment, the workpiece is caused to rotate during the coating operation (par. 49, 1-5; par. 51, 1-5; and par. 91, lines 9-19).

In one embodiment, a flow is produced at least below the workpiece in the electrophoretic resist during the coating operation (par. 49, lines 7-9).

In one embodiment, the electrophoretic resist is caused to rotate in a region of the surface of the workpiece (par. 49, lines 16-18). The rotation of the electrophoretic resist is produced by a stirrer (par. 49, lines 16-18).

The workpiece is removed in a horizontal position after the process of coating with the electrophoretic resist and the coating is baked thermally (par. 112, lines 8-18).

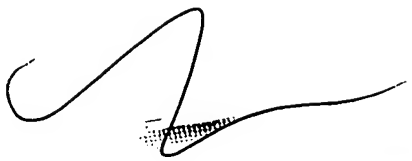
The structure of Brintzinger is a three dimensional (3D) structure (par. 21, lines 1-3). One advantage of using an electrophoretic resist in place of a conventional photoresist is that an electrophoretic resist is useful for depositing a material on 3D structures because it covers highly topographical surfaces with a conformal layer of material (Klocke – par. 31, lines 1-6). Thus, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Brintzinger by using an electrophoretic resist in place of the photoresist, as taught by Klocke, because an electrophoretic resist covers highly topographical surfaces with a conformal layer of material.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
14 May 2005



Mary Wilczewski
Primary Examiner